REMARKS

Claims 1-24 are pending. By this amendment, the Specification and Figures 1-7 are amended. The Figures are amended to overcome the Draftsperson's objections. The Specification is amended to correspond to the amendments made to the Figures. Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached pages are captioned "**Version with markings to show changes made.**" No new matter is introduced. Reconsideration and allowance of the claims in view of the above-amendments and the remarks that follow are respectfully requested.

I. FORMAL MATTERS

Figures 1-7 have been amended to address and overcome the Draftsperson's Objections. In order to address the Draftsperson's for some of the Figures, it was necessary to split Figure into multiple Figures. For example, Figure 2 has been replaced with Figures 2A and 2B, Figure 3 has been replaced with Figures 3A-3C, Figure 4 has been replaced with Figures 4A-4C, Figure 5 has been replaced with Figures 5A-5B, and Figure 6 has been replaced with Figures 6A-6B. In these cases, each replacement Figure shows a portion of the diagram shown by the original Figure. Consequently, it was necessary to amend the Specification to refer to these new replacement Figures.

II. ELECTION/RESTRICTION

Paper No. 3 stated that the application contains claims directed to the following patentably distinct species of the claims invention:

Species I of Figs. 1-4 and 7;

Species II of Figs. 1, 2, and 5; and

Species III of Figs. 1 and 6.

Paper No. 3 also required that the Applicant elect one of these species for prosecution on the merits. Accordingly, Applicants elect the designated Species I of Figs. 1-4 and 7. Claims 1-3 and 5-24 read on Species I. Therefore, the Applicant respectfully requests examination on the merits of claims 1-3 and 5-24 and issuance of a Notice of Allowance. Applicant respectfully requests the Examiner to call Applicant's representative if the Examiner has any questions about the claims of Species I.

III. CONCLUSION

In view of the above, it is respectfully submitted that all claims are in condition for allowance. Applicant respectfully requests allowance of all rejected claims.

A check for $460.00 is submitted herewith for the three-month extension of time. The Commissioner is hereby authorized to charge any additional fees created by this response or credit any overpayment to Deposit Account Number 04-1425. A duplicate copy of this amendment is enclosed for that purpose.

If the Examiner believes that any issues remain unresolved, he is invited to telephone the undersigned to expedite issuance.

Respectfully submitted,

Date: **October 21, 2002**

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Attachments:
1. Drawing Transmittal Letter, including Proposed Replacement Figures 1-7
2. Version With Markings To Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning on page 3, line 12 has been amended as follows:

Figures 2A and 2B are [is] a block diagram of a system for measuring a cable length according to one embodiment of the invention;

The paragraph beginning on page 3, line 14 has been amended as follows:

Figures 3A, 3B and 3C are [is] a schematic diagram of a first circuit according to the invention;

The paragraph beginning on page 3, line 15 has been amended as follows:

Figures 4A, 4B and 4C are [is] a schematic diagram of a second circuit according to the invention;

The paragraph beginning on page 3, line 16 has been amended as follows:

Figures 5A and 5B are [is] a schematic diagram of a third circuit according to the invention;

The paragraph beginning on page 3, line 17 has been amended as follows:

Figures 6A and 6B are [is] a schematic diagram of a fourth circuit according to the invention; and

The paragraph beginning on page 6, line 11 has been amended as follows:

Presented below are four embodiments of a cable length measurement apparatus. Embodiment 1 is described below with reference to a block diagram (Figures 2A-2B) and a circuit schematic (Figures 3A-3C). Embodiments 2-4 are described below with reference to circuit diagrams (Figures 4A-6C). A cable length measurement method is described below with reference to a flow chart (Figure 7). Finally, a suitable for use with the cable length measurement invention, is described in greater detail.

The heading on page 8, line 10 has been amended as follows:

-- Overview of Circuit Components (Figures 3A-3C) –

The paragraph beginning on page 8, line 11 has been amended as follows:

F1 & F3 Generator: A programmable interrupt controller (PIC) microcontroller is programmed to produce two frequencies, which can be called F1 and F3. F1 is passed along

directly as Fa, in this case, correlating to Figures 2A and 2B. F3, however, is produced by dividing F1 down by a factor, N2 where N2 is an integer. This new frequency, F3, enters into the PLL circuit which is wired as a frequency multiplier. Frequency F1 is derived from the 20MHz input clock by dividing it by a relatively large number and multiplying that by a smaller number, resulting in F1 = x1/x2 * 20Mhz.

The paragraph beginning on page 8, line 18 has been amended as follows:

PLL Frequency Multiplier & Divide by N1: The PLL is used to "multiply-up" the incoming F3 frequency by the value "N1" to produce F2, called Fb in Figures 2A and 2B. The result is that F2 is exactly equal to F3 * N1 in the average, but includes a factor of error on a cycle-by-cycle basis, called "jitter." Both characteristics of F2, namely exact average and jitter, are key factors in achieving accurate measurement results.

The paragraph beginning on page 8, line 23 has been amended as follows:

Sample-Hold Latch (Mixer): This device is key to the theory of operation of this circuit, and is a unique application for a Flip-Flop. This device is referred to in Figures 2A and 2B, but may be better explained as a signal mixer, rather than as a "Sample-Hold Latch." It may also be explained as a pulse-width multiplier. The Flip-Flop is receiving two signals very close in frequency (separated in frequency by only a few Hertz – a tiny percentage) but very different in pulse width. The signal with the narrower pulse width is entering into the "D" input and the signal with 50 percent duty cycle is entering into the "CLK" input. The result at the output "Q" is a frequency equal to the "beat frequency" or frequency difference between the two incoming signals – this is similar to the effect a mixer would have. The output pulse width, however, is the product of the smaller pulse width multiplied up by the factor of the longer incoming cycle time divided by the differences in periods between the two incoming signals. For this reason, the Flip-Flop has the effect of multiplying the incoming pulse width up in width, to a more readable duration, where a high-speed counter would not be necessary.

The paragraph beginning on page 9, line 12 has been amended as follows:

Figures 2A and 2B are [is] a block diagram of a system for measuring a cable length, according to Embodiment 1 of the cable length measurement invention. The system is composed of two major sections, the cable-length-controlled pulse width oscillator section and the pulse width testing and data output section, as shown in Figures 2A and 2B. Figures 3A-3C are [is] a schematic diagram of a corresponding circuit.

The paragraph beginning on page 13, line 8 has been amended as follows:

Figures 4A-4C are [is] schematic diagram of a second circuit (Embodiment 2) according to the invention. This circuit and the general operation of this circuit are very similar to Embodiment 1 with the exception that the performance has been improved for shorter cable lengths. With shorter cable lengths applied using the Embodiment 1 circuit, C14 never obtains a charge heavy enough to result in a pulse suitable to clear the U7B flip-flop. That is, when the output of U10 is low for the great majority of the cycle time (short cables), and when it goes high only briefly and then low again, the low-going pulse is too small to be detected by U7B and the circuit does not function properly.

The paragraph beginning on page 14, line 12 has been amended as follows:

Figures 5A and 5B are [is] schematic diagram of a third circuit (embodiment 3) according to the invention. Any "phantom" triggers caused by jitter in the phase-locked-loop circuit can be eliminated by replacing the PLL with two asynchronous crystal controlled oscillators. The problem with the PLL, as with any PLL, is slight jitter in the frequencies. A processor can easily correct the problem by taking many samples and averaging the results, especially after eliminating results that are more than a standard deviation away from the normal. But another method is used in this circuit, where two separate crystals are used.

The paragraph beginning on page 14, line 22 has been amended as follows:

Figures 6A and 6B are [is] schematic diagram of a fourth circuit (Embodiment 4) according to the invention. Embodiment 4 differs from the previous embodiments in that the Length Error indicator has been removed, as well as the initial divide-by-two flip-flop that squares the pulse. As a result, this circuit allows for 1 foot resolution, or 3 ns, using the same F1 and F2 frequencies as before. No length error is provided, so cables must be limited in length or the late return pulses can cause false readings. This circuit provides excellent results for cables known to be no longer than a certain maximum length.

The paragraph beginning on page 15, line 6 has been amended as follows:

Figure 7 is a flow chart of a method according to the invention. The following is a detailed explanation of the two concurrent processes depicted in Figures 6A and 6B. Parenthetical references are made to the elements of the Embodiment 1 circuit (Figures 3A-3C).